Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-12 (cancelled)

Claim 13. (currently amended) A non volatile memory, comprising:

a) flash memory cells organized in rows and columns,

b) cells in a row are interconnected by a word line connecting to control gates of said flash memory cells in said row,

c) cell layout in a first column of cells ~~mirrors~~having a same said cell layout in adjacent second and a third columns of cells, whereby a bit line connects to a select and control portion of a channel of a memory device of said cells in the first column and the bit line connects to a stacked gate portion of said channel of the third column of cells, ~~producing a first pair of adjacent columns with drains close together and a second pair of adjacent columns with sources close together,~~

d) a~~said~~ bit line extends full length of said columns, laying between said cells of said first ~~pair of adjacent~~and third columns, ~~and connecting said drains of said first pair of adjacent columns to a sense amplifier~~,

e) a source line extends full length of said columns, laying between said cells of said first and second columns, whereby said source line connects to a stacked gate

portion of said channel of the first column of cells and the source line connects to a select and control portion of said channel of the second column of cells, ~~second pair of adjacent columns and connecting said sources of said second pair of adjacent columns to source voltages;~~

f) a program operation of said flash memory cells organized by a vertical page comprising said memory cells in the first column ~~associated with said source line,~~ whereby a source line voltage and a bit line voltage of said vertical page are set for said program operation and a word line program voltage is stepped from cell to cell in said first column,

g) an erase operation of said flash memory cells organized by a horizontal block comprising a first row of cells adjacent to a second row of cells and whereby all bit lines, source lines and word lines of said horizontal block are coupled to a same low voltage and then word lines coupled to cells in said horizontal block ~~to be erased~~ are biased to an erase voltage~~;~~,

h) said cell layout in a~~said~~ columns ~~is a same said cell layout in adjacent columns producing a first adjacent column with drains of cells connected to a first source line and sources of cells connected to a first bit line, and a second adjacent column with sources of cells connected to said first source line and drains of cells in said second adjacent column connected to a second bit line,~~ allowing vertical page programming and horizontal page/block erase.

14. (currently amended) The non volatile memory of claim 13 wherein, said bit lines ~~extend full length of said columns, laying between a first pair of adjacent columns, connecting to said drains of a first column of said first pair of adjacent columns, to said sources of a second column of said first pair of adjacent columns, and~~ provide a path to read data stored in said cells ~~connecting to a sense amplifier~~ when performing a read operation.

15. (currently amended) The non volatile memory of claim 13 wherein, said source lines ~~extend full length of said columns, laying between a second pair of adjacent columns,~~ connecting to ~~said~~ sources of said cells of athe first column ~~of said second pair of adjacent columns~~, connecting to ~~said~~ drains of said cells of the second column ~~second pair of adjacent columns~~, and connecting to source voltages.

Claims 16-25 (canceled)